

## CLAIMS

What is claimed is:

1 1. An integrated circuit fabricated on a chip, comprising:  
2 an on-chip logic analyzer;  
3 a cache memory that includes a plurality of cache sets;  
4 at least one on-chip logic device that stores data to said plurality of cache sets during  
5 normal operation; and  
6 a logic gate that receives an enable signal when the on-chip logic analyzer is enabled, and  
7 which disables at least one of said plurality of said cache sets for storing data from said on-chip  
8 logic analyzer.

1 2. The system of claim 1, wherein the integrated circuit comprises a processor, and the on-  
2 chip logic device includes a CPU core.

1 3. The system of claim 2, wherein the enable signal is generated by the on-chip logic  
2 analyzer.

1 4. The system of claim 3, wherein the logic comprises a multiplexer that connects the on-chip  
2 logic analyzer to the disabled cache set when the on-chip logic analyzer asserts the enable signal.

1 5. The system of claim 4, wherein the multiplexer forms part of a cache controller.

1 6. The system of claim 1, wherein the on-chip logic analyzer receives information regarding  
2 internal state data of the processor and selects some of the received information for storage in the  
3 disabled cache set.

1 7. The system of claim 6, further comprising a second on-chip logic analyzer that receives  
2 information regarding instructions executing in the processor, and wherein the second on-chip  
3 logic analyzer selects at least some of said received information for storage in the disabled cache  
4 set.

1 8. The system of claim 7, wherein the disabled cache set is sub-divided into multiple portions,  
2 and said on-chip logic analyzer and said second on-chip logic analyzer are each assigned a portion  
3 of said disabled cache set.

1 9. The system of claim 1, further comprising a cache controller that couples to said cache  
2 memory and which controls accesses to said cache memory, and wherein data stored by the on-  
3 chip logic analyzer is assigned an address range, and said cache controller forces a hit on said  
4 disabled cache set when a read request is made to the address range assigned to the on-chip logic  
5 analyzer.

1 10. The system of claim 1, wherein data stored by the on-chip logic analyzer is assigned an  
2 address range, and said disabled cache set makes available at least a portion of the data stored  
3 therein when a read request is made to the address range assigned to the on-chip logic analyzer.

1 11. The system of claim 10, wherein the on-chip logic analyzer includes an addressable read  
2 register that receives data stored in the disabled cache set in response to a read request to an  
3 address range assigned to the on-chip logic analyzer.

1 12. A processor, comprising:  
2 a CPU core;  
3 a cache memory coupled to said CPU core, said cache memory including a plurality of  
4 cache sets that during normal operation store data written by the CPU core; and  
5 at least one logic analyzer that receives information relating to the internal state of the  
6 processor, said logic analyzer being coupled to at least one of said plurality of cache sets, and  
7 wherein said logic analyzer is capable of gaining ownership of said at least one cache set to store  
8 selected portions of said received information when said on-chip logic analyzer is enabled.

1 13. The processor of claim 12, further comprising a multiplexer that couples to said CPU core  
2 via a first bus and which couples to said logic analyzer via a second bus, and wherein said  
3 multiplexer selects either said first bus or said second bus to connect to said at least one cache set.

1 14. The processor of claim 13, wherein said multiplexer receives an enable signal indicating  
2 whether to connect said first bus or said second bus to said at least one cache set.

1 15. The processor of claim 13, wherein the logic analyzer is located on-chip.



3 test logic coupled to said cache memory, which tests the cache sets during system  
4 initialization and determines which cache sets are operative;

5 a cache controller that controls the storage and retrieval of data from said cache memory,  
6 with said cache controller only storing data to cache sets that are determined to be operative by the  
7 test logic;

8 a CPU core coupled to said cache memory, said CPU core storing data to all operative  
9 cache sets during normal operation;

10 an on-chip logic analyzer capable of receiving data reflecting the internal state of the  
11 processor, said on-chip logic analyzer coupled to at least one cache set, which is disabled from use  
12 by the CPU core when the on-chip logic analyzer is enabled.

1 22. The processor of claim 21, wherein data stored by the on-chip logic analyzer is assigned an  
2 address range, and said cache controller forces a hit on said disabled cache set when a read request  
3 is issued to the address range assigned to the on-chip logic analyzer.

1 23. The processor of claim 22, wherein the on-chip logic analyzer includes an addressable read  
2 register that receives data stored in the disabled cache set in response to the read request to an  
3 address range assigned to the on-chip logic analyzer.

1 24. The processor of claim 21, wherein the on-chip logic analyzer is capable of issuing a read  
2 request to the cache controller for data stored in the disabled cache set, which includes a signal  
3 indicating that the cache controller should force a hit on the disabled cache set.

1 25. A method of maintaining state data of a processor in a cache memory set, comprising the  
 2 acts of:  
 3 enabling an on-chip logic analyzer to receive and select data for storage;  
 4 disabling a cache set from use by any device other than the on-chip analyzer;  
 5 storing said selected data in the disabled cache set.

1 26. The method of claim 25, further comprising the acts of:  
 2 reading said selected data from said disabled cache set; and  
 3 storing said data read from the disabled cache set to an addressable register.

1 27. The method of claim 25, wherein the act of disabling the cache set includes transmitting an  
 2 enable signal to a multiplexer that selects the on-chip logic analyzer as the sole source of data to be  
 3 written to the cache set.

1 28. The method of claim 26, wherein the act of reading selected data includes:  
 2 issuing a read request to an I/O address reserved for on-chip logic analyzer data;  
 3 recognizing the read request as targeting on-chip logic analyzer data;  
 4 routing the read request to the cache memory; and  
 5 forcing a hit on the disabled cache set.

1 29. The processor of claim 17, wherein said test logic will preserve the contents of at least one  
 2 said cache set during a reset operation if said first enable signal is asserted.